REMARKS

The Office Action of September 13, 2011 was received and carefully reviewed. Claims 6, 8-14, 17-22, 24-27, 29, 47-50 and 55-59 were pending in this application prior to the instant amendment. By this amendment, claims 6, 12, 18, 24, 55 and 57 are amended, new claims 60 and 61 are added, and claims 56 and 58 are canceled without prejudice or disclaimer. No new matter has been added. Thus, claims 6, 8-14, 17-22, 24-27, 29, 47-50 and 55, 57, 59-61 remain currently pending for consideration.

Claim Rejections Under 35 U.S.C. § 103

Claims 18, 19, 22 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,471,225 to Parks ("Parks"), in view of Japanese Pat. App. Pub. No. JP 58-143389 to Hoshi ("Hoshi"). Claims 6, 8, 11, 47 and 55-59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Parks, in view of U.S. Patent No. 5,325,338 to Runaldue et al. ("Runaldue"), and further in view of Hoshi. Claims 9 and 10 stand rejected under § 103(a) as being unpatentable over Parks in view of Runaldue, and further in view of Hoshi and U.S. Patent No. 5,196,839 to Johary et al. ("Johary"). Claims 12-14, 17, 20, 21, 24-27, 29, 48 and 50 stand rejected under § 103(a) as being unpatentable over Parks in view of Hoshi, and further in view of Johary. These rejections are traversed for at least the reasons advanced in detail below.

Applicant continuous to contend that the embodiments of the invention recited in the currently pending claims include a combination of features that are not disclosed by the cited references noted above for the reasons advanced in detail below and in the Amendment filed August 12, 2010, those reasons being incorporated herein by reference. Turning to the Office Action of September 13, 2011, on page 2 of thereof, the Examiner asserts that the signal selection circuit of Hoshi can be broadly read as part of a digital memory circuit which includes said selection circuit and the memory cell. (id.). Further, the Examiner states that because it is unclear what specific components are included in the claimed memory circuit, such memory circuit is "seen as being capable of being read to reasonably include both the memory cell and selection circuit of Hoshi." (*See, sentence bridging pages 2-3 of the Office Action.*). In addition, the Examiner cites Hoshi to fill in the features Parks fails to disclose, that is "providing an AC voltage to the opposite electrode or that the AC voltage has the same amplitude as the voltage supplied to the pixel electrode from the memory circuit." Moreover, the Examiner cites Runaldue for allegedly teaching "a display memory circuit which comprises a pair of inverters connected to each other (100-103 in FIG. 3, Runaldue), each of said inverters comprising an N-channel TFT (101 and 103 in FIG. 3, Runaldue) and a P-channel TFT (100 and 102 in FIG. 3,

Runaldue)." (*See, page 7 of the Office Action*). As a result, the Examiner concludes it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption. (See, page 8 of the Office Action). Applicant respectfully disagrees.

Without conceding in detail the merits of the Examiner's rejections, Applicant herein amends independent claim 1 to recite, *inter alia*,

> "wherein the memory circuit comprises a pair of inverters, each of the inverters comprising an n-channel thin film transistor and a p-channel thin film transistor, wherein an input of one of the pair of inverters is connected to the thin film transistor and an output of the other one of the pair of inverters, and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and one of the plurality of pixel electrodes."

Similar amendments have been made in independent claims 18, 55 and 57. Further, Applicant herein amends independent claim 24 to recite, *inter alia*,

> "wherein the memory circuit comprises at least second and third thin film transistors, one of source or drain of the second thin film transistor being connected with one of the two voltage source lines through a first resistor, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,
>
> the other of source or drain of the second transistor being connected with the other of the two voltage source lines and one of source or drain of the third thin film transistor, and
>
> a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, the one of the two voltage source lines through a second resistor, and the pixel electrode."

Applicant submits that independent claim 12 recites features similar to that of claim 24 with respect to the memory circuit as indicated above. Support for the above-noted features can be found, for example, FIG. 8 of U.S. Patent No. 5,798,746 ("'746 patent) from which the instant application claims a priority benefit.

Applicant continues to contend that Parks, Hoshi, Runaldue and/or Johary, taken alone or in combination, fail to disclose, suggest or render obvious independent claims 6, 12, 18, 24, 55 and 57, particularly in light of the above features. For example, the memory cell 7 and the selection circuit 8 shown in FIG. 2 (alleged by the Examiner to correspond the claimed memory circuit) disclosed on page 4, line 6, and lines 17-21 of Hoshi (English translation) states that the memory cell 7 is formed by a flip-flop and the signal selection circuit 8 uses a signal received from common electrode driven by the clock source 10 as an input signal and a signal output from the memory cell 7 as a control signal to selectively output a signal "in-phase" or a signal "in opposite-phase" with the input signal to a liquid crystal cell 9/pixel electrode 9a. Although, Hoshi discloses two inverters 14 and 15 in FIGs. 4-6, these inverters are used to form a flip-flop for the memory cell and require either "exclusive OR" or "two transmission gates" in order to selectively output the signal to the pixel electrode 9a. (*See, for example, page 7, lines 7-10 and lines 16-22, and page 8, lines 1-15, Hoshi*). On the other hand, the claimed invention uses a pair

of inverters and does not require two separate components, namely the memory cell formed of a flip-flop and the signal selection circuit formed of exclusive OR, transmission gates, etc. to output a desired signal to the pixel electrode.

With respect to Runaldue, the memory cell 90 shown in FIG. 3 includes a single-ended port 106 and a differential port 117, where the single-ended port 106 is clocked much faster speed than the differential port 117 to output a video signal which eventually becomes a desired signal for displaying image. On the other hand, the differential port 117 is used to inspect and change the colors represented in the color lookup table 15 shown in FIG. 15 by forming a CPU access port/path. Applicant respectfully submits that the pair of inverters 94 and 98 in the memory cell 90 shown in FIG. 3 of Runaldue (alleged by the Examiner as corresponding the claimed pair of inverters) is actually a part of a differential port 117 that is specifically designed for the CPU access port/path for the purposes discussed above, where the CPU access port/path is clocked at a slower speed than the single-ended port 106. (*See, for example, Abstract and col. 7, lines 36-54, Runaldue*).

Thus, Applicant respectfully submits that a combination of Parks with Hoshi, and Parks with Hoshi and Runaldue would fail to disclose the above discussed features of the claimed invention. Johary, cited as allegedly disclosing a time gradation display device, also fail to overcome the above noted deficiency of Runaldue and Hoshi.

In view of above, a *prima facie* case of obviousness cannot be maintained. Thus, Applicant respectfully requests reconsideration and withdrawal of the rejection of independent claims 6, 12, 18, 24, 55 and 57. The rejection of dependent claims 8-11, 13, 14, 17, 19-22, 25-27, 29, 47-50 and 59 is believed to be improper at least by virtue of their dependency on claims 6, 12, 18, 24, 55 or 57. The rejection of claims 56 and 58 is rendered moot by virtue of their cancellation herein.

CONCLUSION

Accordingly, Applicant respectfully requests reconsideration and allowance of the instant application. If a conference would be helpful in expediting prosecution of the instant application, the Examiner is invited to telephone the undersigned to arrange such a conference.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account

No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

NIXON PEABODY, LLP

/Jeffrey L. Costellia, Reg.#35,483/
Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
CUSTOMER NO.: 22204
401 9th Street, N.W., Suite 900
Washington, DC 20004
Tel: 202-585-8000